CY7C199D Automotive

256-Kbit (32K × 8) Static RAM

Features

- Temperature ranges
  - Automotive-E: –40 °C to 125 °C
- Operating voltage V_{CC} = 5 V
- Pin and function compatible with CY7C199C
- High speed
  - t_{AA} = 25 ns
- Low active power
  - I_{CC} = 63 mA
- Low complementary metal oxide semiconductor (CMOS) standby power
  - I_{SB2} = 15 mA
- 2.0 V Data Retention
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Pb-free 28-pin 300-Mil-wide small-outline integrated circuit (SOIC)

Functional Description

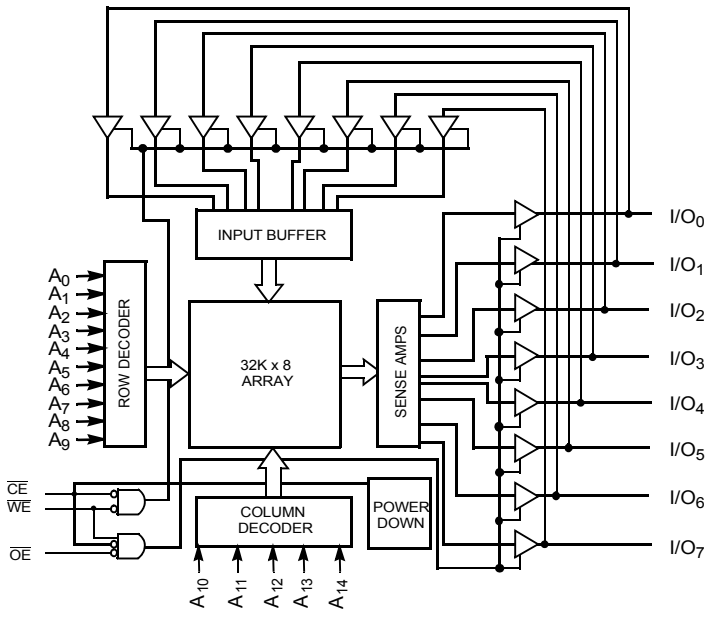
The CY7C199D Automotive is a high performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$) and tri-state drivers. This device has an automatic power-down feature, reducing the power consumption when deselected. The input and output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Write to the device by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{14}).

Read from the device by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the I/O pins.

For a complete list of related resources, click here.

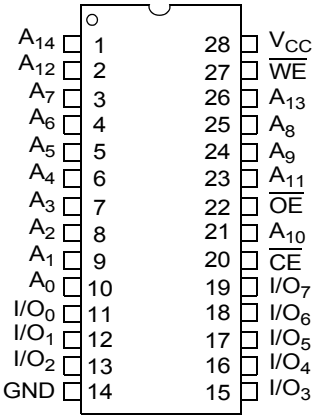
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 28-pin SOIC pinout (Top View)



Selection Guide

Description	-25 (Automotive) [1]	Unit
Maximum access time	25	ns
Maximum operating current	63	mA
Maximum CMOS standby current	15	mA

Note
1. Automotive product information is preliminary.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND [2] .....–0.5 V to +6.0 V

DC voltage applied to outputs in High Z State [2] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage [2] ..... –0.5 V to V_{CC} + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2,001 V

Latch-up current ..... > 140 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Automotive-E	–40 °C to +125 °C	5 V ± 0.5 V	25 ns

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions		CY7C199D Automotive-25		Unit
				Min	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output LOW voltage	I_{OL} = 8.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage [2]	–		2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage [2]	–		–0.5	0.8	V
I_{IX}	Input leakage current	$GND \le V_I \le V_{CC}$		–5	+5	µA
I_{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$, output disabled		–5	+5	µA
I_{CC}	V_{CC} operating supply current	$V_{CC} = V_{CC(max)}$, I_{OUT} = 0 mA, $f = f_{max} = 1/t_{RC}$	40 MHz	–	63	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	$V_{CC} = V_{CC(max)}$, $\overline{CE} \ge V_{IH}$, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, f = f_{max}		–	50	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	$V_{CC} = V_{CC(max)}$, $\overline{CE} \ge V_{CC}$ – 0.3 V, $V_{IN} \ge V_{CC}$ – 0.3 V or $V_{IN} \le$ 0.3 V, f = 0		–	15	mA

Note
2. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)} = V_{CC}$ + 1 V for pulse durations of less than 5 ns.

Capacitance

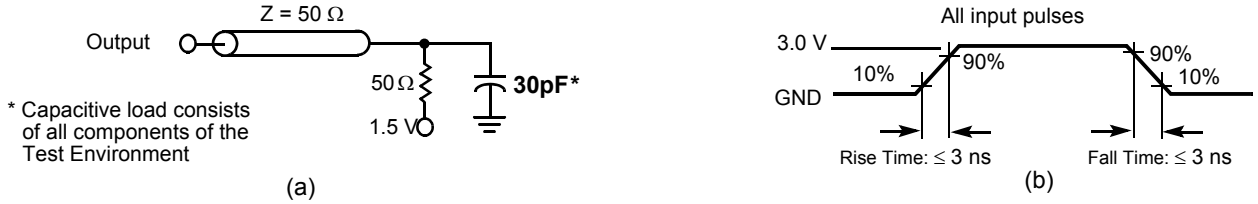
Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

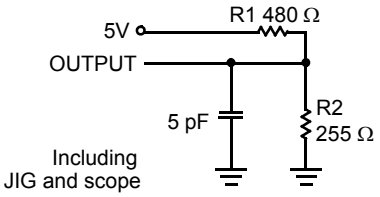
Parameter [3]	Description	Test Conditions	28-pin SOIC [4]	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	54.05	°C/W
Θ_{JC}	Thermal resistance (junction to case)		27.44	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [5]



High Z characteristics:



Notes
3. Tested initially and after any design or process changes that may affect these parameters.
4. Automotive product information is preliminary.
5. AC characteristics (except High Z) are tested using the load conditions shown in Figure 2 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

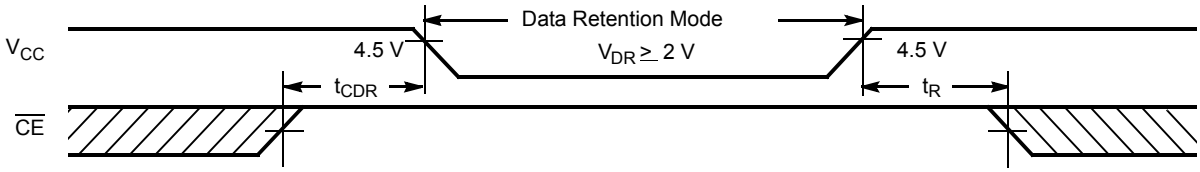
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	–	15	mA
t_{CDR} [6]	Chip deselect to data retention time		0	–	ns
t_R [7]	Operation recovery time		25	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.

Switching Characteristics

Over the operating range

Parameter [8]	Description	CY7C199D Automotive-25		Unit
		Min	Max	
Read Cycle				
t_{power} [9]	$V_{CC(typical)}$ to the first access	100	–	µs
t_{RC}	Read cycle time	25	–	ns
t_{AA}	Address to data valid	–	25	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	25	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	11	ns
t_{LZOE} [10]	$\overline{OE}$ LOW to Low Z	0	–	ns
t_{HZOE} [10, 11]	$\overline{OE}$ HIGH to High Z	–	11	ns
t_{LZCE} [10]	$\overline{CE}$ LOW to Low Z	3	–	ns
t_{HZCE} [10, 11]	$\overline{CE}$ HIGH to High Z	–	11	ns
t_{PU} [12]	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD} [12]	$\overline{CE}$ HIGH to power-down	–	25	ns
Write Cycle [13, 14]				
t_{WC}	Write cycle time	25	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	18	–	ns
t_{AW}	Address setup to write end	18	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ LOW to write end	18	–	ns
t_{SD}	Data setup to write end	12	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE} [10]	$\overline{WE}$ LOW to High Z	–	11	ns
t_{LZWE} [10, 11]	$\overline{WE}$ HIGH to Low Z	3	–	ns

Notes

8. Test conditions assume signal transition time of 3 ns or less for all speeds, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
11. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of Figure 2 on page 5. Transition is measured ±200 mV from steady-state voltage.
12. This parameter is guaranteed by design and is not tested.
13. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
14. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [15, 16]

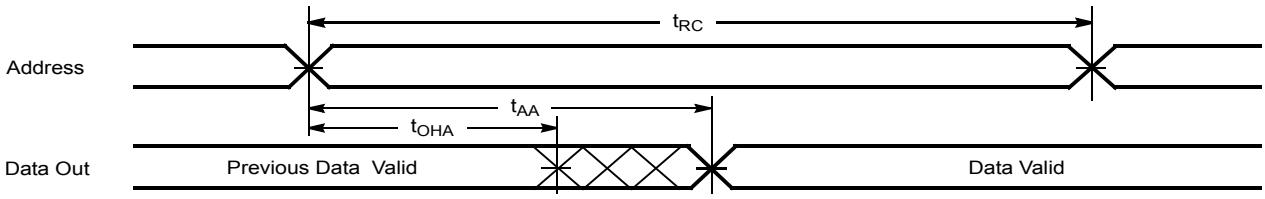
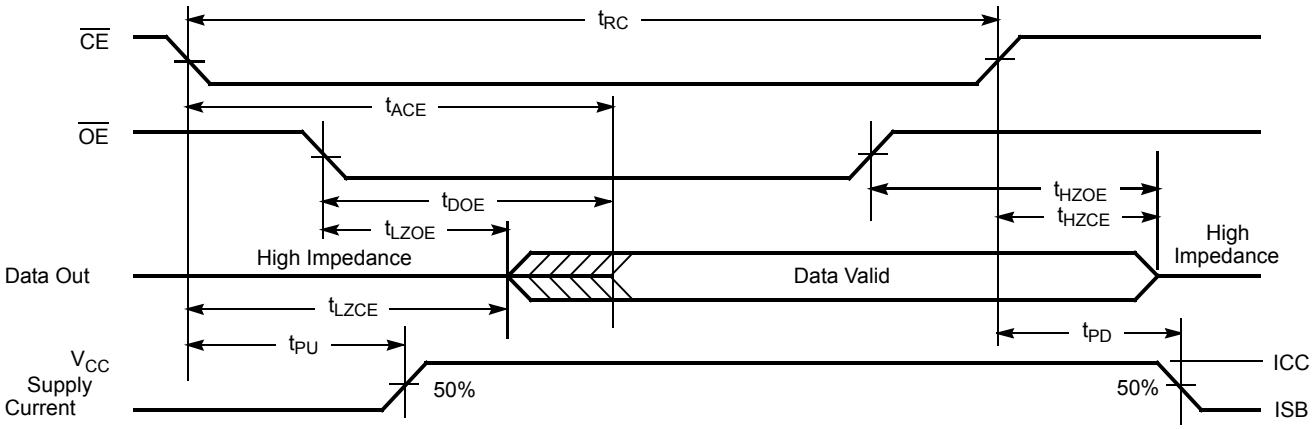


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [16, 17]



Notes
15. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
16. $\overline{WE}$ is HIGH for read cycle.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms *(continued)*

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [18, 19]

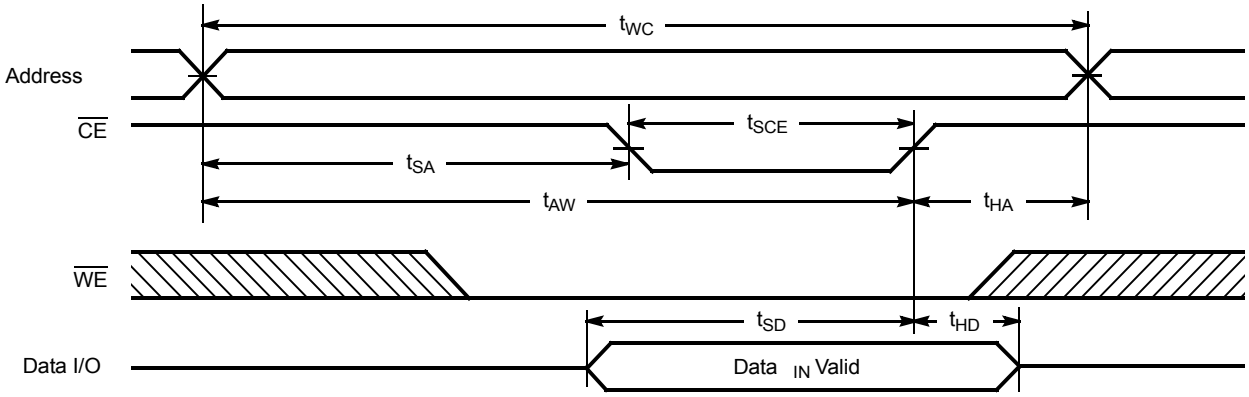
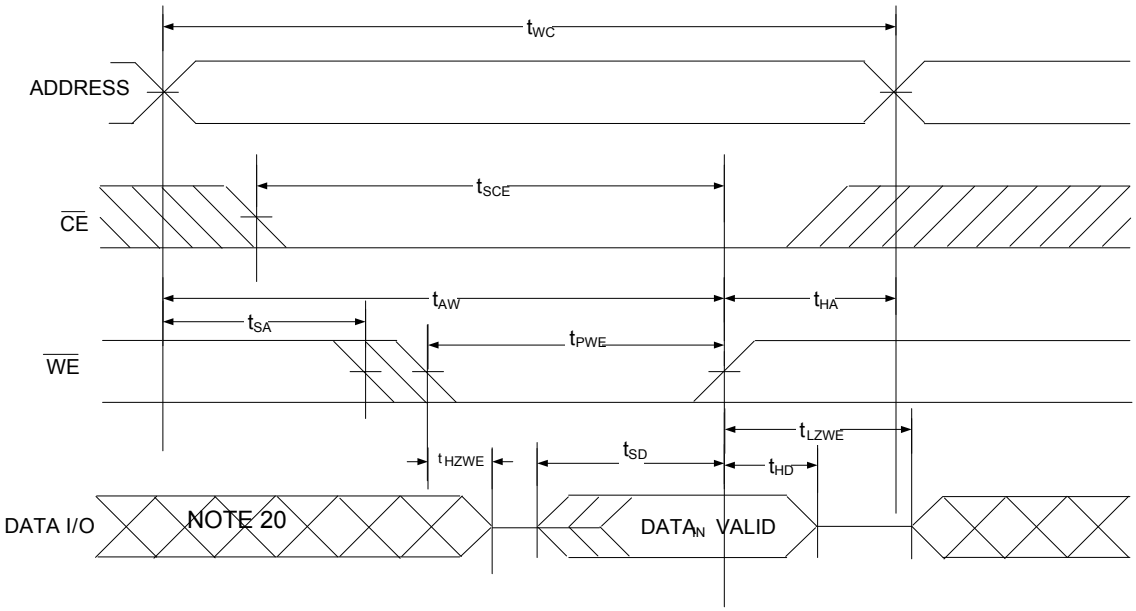


Figure 7. Write Cycle No. 2 ($\overline{WE}$ Controlled) [18, 19]

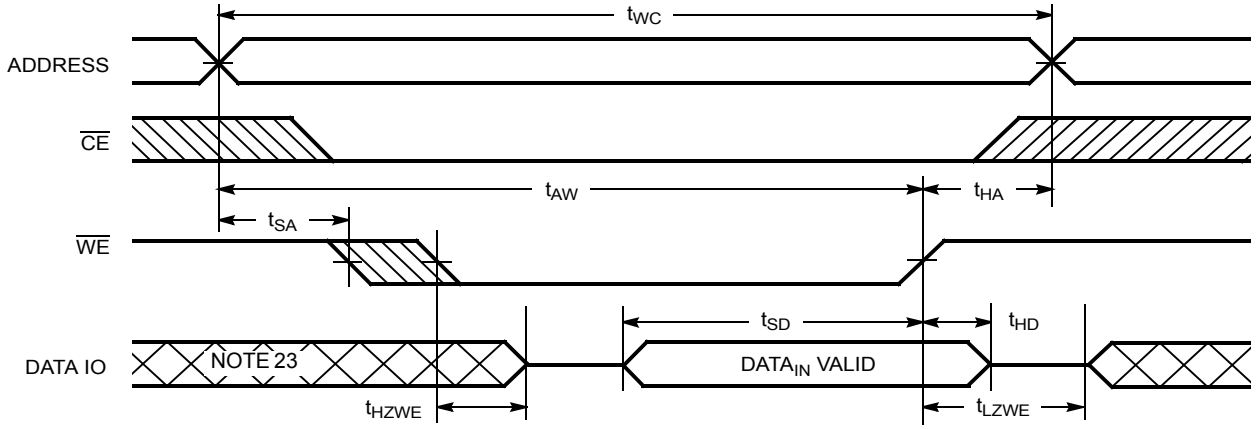


Notes

18. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
19. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
20. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms *(continued)*

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [21, 22]



Notes
21. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
22. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
23. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})
L	H	H	High Z	Deselect, output disabled	Active (I_{CC})

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at http://www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

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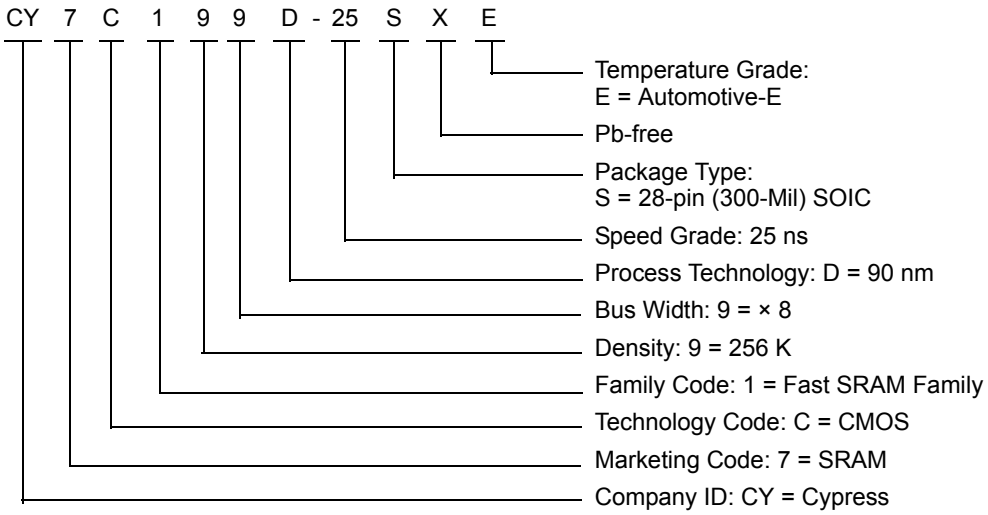
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY7C199D-25SXE	51-85026	28-pin (300-Mil) SOIC (Pb-free)	Automotive-E [24]

Please contact your local Cypress sales representative for availability of these parts.

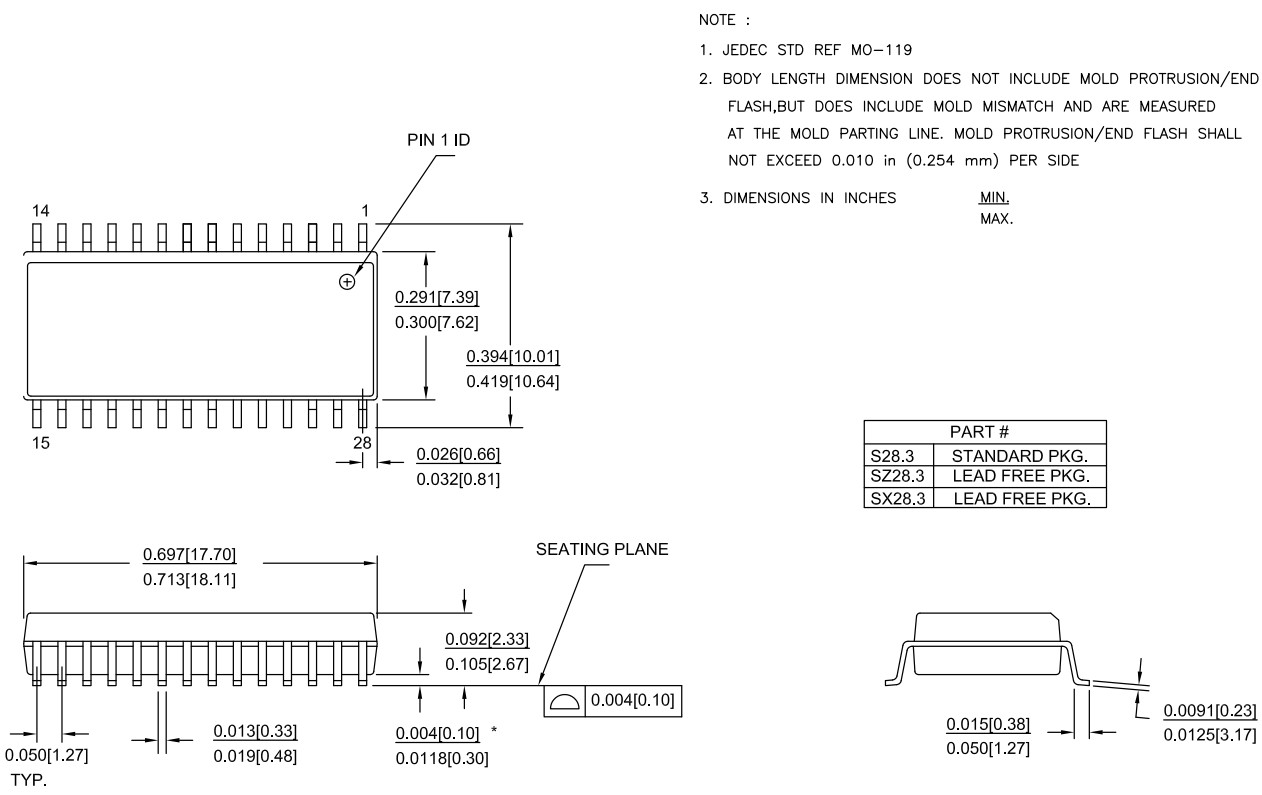
Ordering Code Definitions



Note
24. Automotive product information is preliminary.

Package Diagrams

Figure 9. 28-pin (300-Mil) SOIC (0.713 × 0.300 × 0.0932 Inches) Package Outline, 51-85026



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SOIC	Small-Outline Integrated Circuit
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C199D Automotive, 256-Kbit (32K × 8) Static RAM Document Number: 001-65330				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3124050	PRAS	01/07/2011	New datasheet - Auto info removal from the 199D Industrial datasheet
*A	3270574	PRAS	05/31/2011	Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated Package Diagrams.
*B	3890204	MEMJ	02/01/2013	Updated Features: Added “Operating voltage V_{CC} = 5 V”. Updated Thermal Resistance: Replaced TBD with 54.05 for Θ_{JA}. Replaced TBD with 27.44 for Θ_{JC}. Updated Switching Characteristics: Updated description of t_{PWE} parameter. Removed the Note “The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.” and its references. Updated Switching Waveforms: Updated Figure 7 (Removed redundant information of t_{HZOE} and $\overline{OE}$ from the diagram). Removed the Figure “Write Cycle No. 3 $\overline{WE}$ Controlled, $\overline{OE}$ LOW”. Removed the Note “Data I/O is high impedance if $\overline{OE}$ = V_{IH}.” and its references. Removed the Note “The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.” and its references.
*C	3961032	TAVA	04/10/2013	Changed status from Preliminary to Final.
*D	4755186	PSR	05/05/2015	Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Updated Package Diagrams: spec 51-85026 – Changed revision from *F to *H. Updated to new template.
*E	5144461	VINI	02/19/2016	Updated Switching Characteristics: Added Note 14 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Figure 8. Updated to new template. Completing Sunset Review.

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