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R8C/2K Group, R8C/2L Group RENESAS MCU

REJ03B0219-0110 Rev.1.10 Dec 21, 2007

1. Overview

1.1 Features

The R8C/2K Group and R8C/2L Group of single-chip MCUs incorporates the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI. Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

Furthermore, the R8C/2L Group has on-chip data flash (1 KB \times 2 blocks).

The difference between the R8C/2K Group and R8C/2L Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.



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1.1.2 Specifications

Tables 1.1 and 1.2 outlines the Specifications for R8C/2K Group and Tables 1.3 and 1.4 outlines the Specifications for R8C/2L Group.

Table 1.1 Specifications for R8C/2K Group (1)

Item	Function	Specification
CPU	Central processing	R8C/Tiny series core
	unit	Number of fundamental instructions: 89
		Minimum instruction execution time:
		50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)
		100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
		200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)
		Multiplier: 16 bits × 16 bits → 32 bits
		 Multiply-accumulate instruction: 16 bits x 16 bits + 32 bits → 32 bits
		Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to Table 1.5 Product List for R8C/2K Group.
Power Supply	Voltage detection	Power-on reset
Voltage	circuit	Voltage detection 3
Detection		
I/O Ports	Programmable I/O	Input-only: 3 pins
	ports	CMOS I/O ports: 25, selectable pull-up resistor
		High current drive ports: 8
Clock	Clock generation	2 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),
	circuits	On-chip oscillator (high-speed, low-speed)
		(high-speed on-chip oscillator has a frequency adjustment function)
		Oscillation stop detection: XIN clock oscillation stop detection function
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16
		• Low power consumption modes:
		Standard operating mode (high-speed clock, high-speed on-chip oscillator,
		low-speed on-chip oscillator), wait mode, stop mode
Interrupts		External: 4 sources, Internal: 15 sources, Software: 4 sources
monapio		Priority levels: 7 levels
Watchdog Tim	er	15 bits × 1 (with prescaler), reset start selectable
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler)
111101		Timer mode (period timer), pulse output mode (output level inverted every
		period), event counter mode, pulse width measurement mode, pulse period
		measurement mode
	Timer RB	8 bits x 1 (with 8-bit prescaler)
		Timer mode (period timer), programmable waveform generation mode (PWM
		output), programmable one-shot generation mode, programmable wait one-
		shot generation mode
	Timer RC	16 bits x 1 (with 4 capture/compare registers)
		Timer mode (input capture function, output compare function), PWM mode
		(output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers)
		Timer mode (input capture function, output compare function), PWM mode
		(output 6 pins), reset synchronous PWM mode (output three-phase
		waveforms (6 pins), sawtooth wave modulation), complementary PWM mode
		(output three-phase waveforms (6 pins), triangular wave modulation), PWM3
		mode (PWM output 2 pins with fixed period)

Table 1.2 Specifications for R8C/2K Group (2)

Item	Function	Specification
Serial	UARTO, UART2	Clock synchronous serial I/O/UART x 2
Interface		
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution x 9 channels, includes sample and hold function
Flash Memory		 Programming and erasure voltage: VCC = 2.7 to 5.5 V
		Programming and erasure endurance: 100 times
		Program security: ROM code protect, ID code check
		Debug functions: On-chip debug, on-board flash rewrite function
Operating Freq	uency/Supply	f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V)
Voltage		f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V)
		f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V) (VCC = 2.7 to 5.5 V for A/D converter only)
Current consur	nption	Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
		Typ. 6 mA (\dot{V} CC = 3.0 V, \dot{f} (\dot{X} IN) = 10 MHz)
		Typ. 23 μA (VCC = 3.0 V, wait mode, low-speed on-chip oscillator used) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Operating Amb	ient Temperature	-20 to 85°C (N version)
Operating / triblent remperature		-40 to 85°C (D version) ⁽¹⁾
		-20 to 105°C (Y version) ⁽²⁾
		32-pin LQFP
l		Package code: PLQP0032GB-A (previous code: 32P6U-A)
		i , , , , , , , , , , , , , , , , , , ,

- 1. Specify the D version if D version functions are to be used.
- 2. Please contact Renesas Technology sales offices for the Y version.

Table 1.3 Specifications for R8C/2L Group (1)

Item	Function	Specification
CPU	Central processing	R8C/Tiny series core
	unit	Number of fundamental instructions: 89
		Minimum instruction execution time:
		50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)
		100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
		200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)
		Multiplier: 16 bits × 16 bits → 32 bits
		 Multiply-accumulate instruction: 16 bits x 16 bits + 32 bits → 32 bits
		Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to Table 1.6 Product List for R8C/2L Group.
Power Supply	Voltage detection	Power-on reset
Voltage	circuit	Voltage detection 3
Detection		
I/O Ports	Programmable I/O	Input-only: 3 pins
	ports	CMOS I/O ports: 25, selectable pull-up resistor
		High current drive ports: 8
Clock	Clock generation	2 circuits: XIN clock oscillation circuit (with on-chip feedback resistor),
	circuits	On-chip oscillator (high-speed, low-speed)
		(high-speed on-chip oscillator has a frequency adjustment function)
		Oscillation stop detection: XIN clock oscillation stop detection function
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16
		• Low power consumption modes:
		Standard operating mode (high-speed clock, high-speed on-chip oscillator,
		low-speed on-chip oscillator), wait mode, stop mode
Interrupts		External: 4 sources, Internal: 15 sources, Software: 4 sources
into in apto		Priority levels: 7 levels
Watchdog Tim	er	15 bits × 1 (with prescaler), reset start selectable
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler)
111101		Timer mode (period timer), pulse output mode (output level inverted every
		period), event counter mode, pulse width measurement mode, pulse period
		measurement mode
	Timer RB	8 bits x 1 (with 8-bit prescaler)
		Timer mode (period timer), programmable waveform generation mode (PWM
		output), programmable one-shot generation mode, programmable wait one-
		shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers)
		Timer mode (input capture function, output compare function), PWM mode
		(output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers)
		Timer mode (input capture function, output compare function), PWM mode
		(output 6 pins), reset synchronous PWM mode (output three-phase
		waveforms (6 pins), sawtooth wave modulation), complementary PWM mode
		(output three-phase waveforms (6 pins), triangular wave modulation), PWM3
		mode (PWM output 2 pins with fixed period)

Specifications for R8C/2L Group (2) Table 1.4

Item	Function	Specification
Serial	UARTO, UART2	Clock synchronous serial I/O/UART x 2
Interface	,	
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 9 channels, includes sample and hold function
Flash Memory		Programming and erasure voltage: VCC = 2.7 to 5.5 V
		 Programming and erasure endurance: 10,000 times (data flash)
		1,000 times (program ROM)
		Program security: ROM code protect, ID code check
		Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V) f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V) (VCC = 2.7 to 5.5 V for A/D converter only)
Current consu	mption	Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 23 μ A (VCC = 3.0 V, wait mode, low-speed on-chip oscillator used) Typ. 0.7 μ A (VCC = 3.0 V, stop mode)
Operating Ambient Temperature -20 to 85°C (N version) -40 to 85°C (D version)(1) -20 to 105°C (Y version)(2)		
Package		32-pin LQFP • Package code: PLQP0032GB-A (previous code: 32P6U-A)

- 1. Specify the D version if D version functions are to be used.
- 2. Please contact Renesas Technology sales offices for the Y version.

1.2 Product List

Table 1.5 lists the Product List for R8C/2K Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2K Group, Table 1.6 lists the Product List for R8C/2L Group, and Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2L Group.

Table 1.5 Product List for R8C/2K Group

Current of Dec. 2007

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F212K2SNFP	8 Kbytes	1 Kbyte	PLQP0032GB-A	N version
R5F212K4SNFP	16 Kbytes	1.5 Kbytes	PLQP0032GB-A	
R5F212K2SDFP	8 Kbytes	1 Kbyte	PLQP0032GB-A	D version
R5F212K4SDFP	16 Kbytes	1.5 Kbytes	PLQP0032GB-A	
R5F212K2SNXXXFP (D)	8 Kbytes	1 Kbyte	PLQP0032GB-A	N version
R5F212K4SNXXXFP (D)	16 Kbytes	1.5 Kbytes	PLQP0032GB-A	Factory programming product ⁽¹⁾
R5F212K2SDXXXFP (D)	8 Kbytes	1 Kbyte	PLQP0032GB-A	D version
R5F212K4SDXXXFP (D)	16 Kbytes	1.5 Kbytes	PLQP0032GB-A	Factory programming product ⁽¹⁾

(D): Under development

NOTE:

1. The user ROM is programmed before shipment.

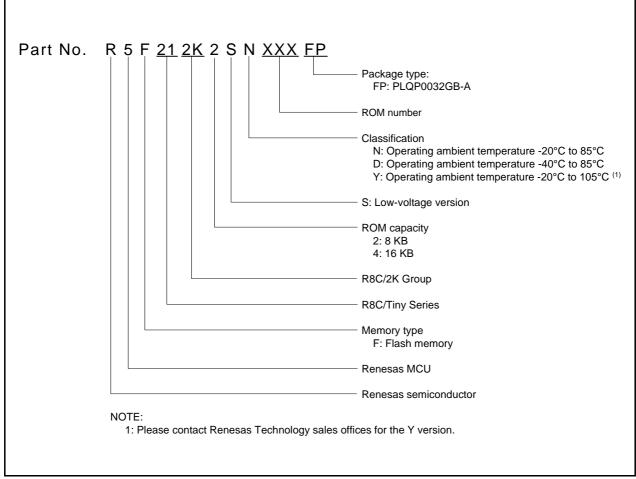


Figure 1.1 Part Number, Memory Size, and Package of R8C/2K Group

Table 1.6 Product List for R8C/2L Group

Current of Dec. 2007

Part No.	ROM Capacity		RAM	Package Type	Remarks
- arriver	Program ROM	Data flash	Capacity	r donago rypo	rtomanto
R5F212L2SNFP	8 Kbytes	1 Kbyte x 2	1 Kbyte	PLQP0032GB-A	N version
R5F212L4SNFP	16 Kbytes	1 Kbyte x 2	1.5 Kbytes	PLQP0032GB-A	
R5F212L2SDFP	8 Kbytes	1 Kbyte x 2	1 Kbyte	PLQP0032GB-A	D version
R5F212L4SDFP	16 Kbytes	1 Kbyte x 2	1.5 Kbytes	PLQP0032GB-A	
R5F212L2SNXXXFP (D)	8 Kbytes	1 Kbyte x 2	1 Kbyte	PLQP0032GB-A	N version
R5F212L4SNXXXFP (D)	16 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A	Factory programming product ⁽¹⁾
R5F212L2SDXXXFP (D)	8 Kbytes	1 Kbyte x 2	1 Kbyte	PLQP0032GB-A	D version
R5F212L4SDXXXFP (D)	16 Kbytes	1 Kbyte × 2	1.5 Kbytes	PLQP0032GB-A	Factory programming product ⁽¹⁾

(D): Under development

NOTE:

1. The user ROM is programmed before shipment.

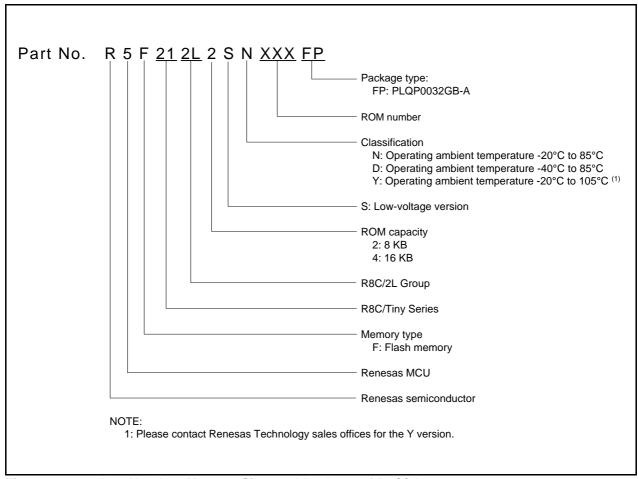


Figure 1.2 Part Number, Memory Size, and Package of R8C/2L Group

1.3 Block Diagram

Figure 1.3 shows a Block Diagram.

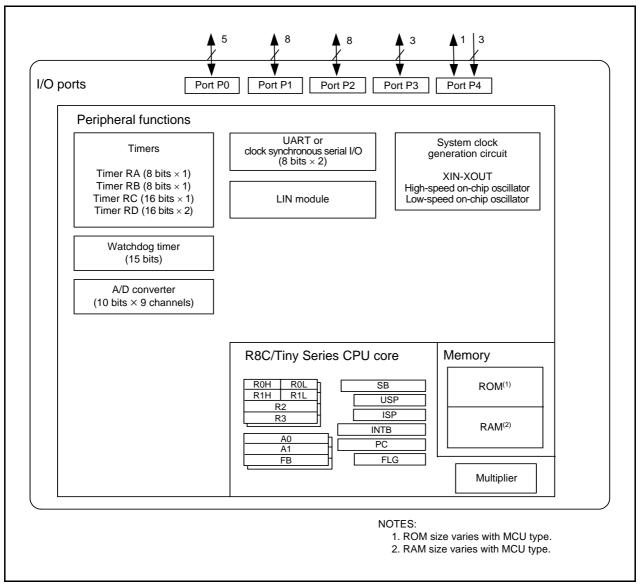


Figure 1.3 Block Diagram

1.4 Pin Assignment

Figure 1.4 shows the Pin Assignment (Top View). Table 1.7 outlines the Pin Name Information by Pin Number.

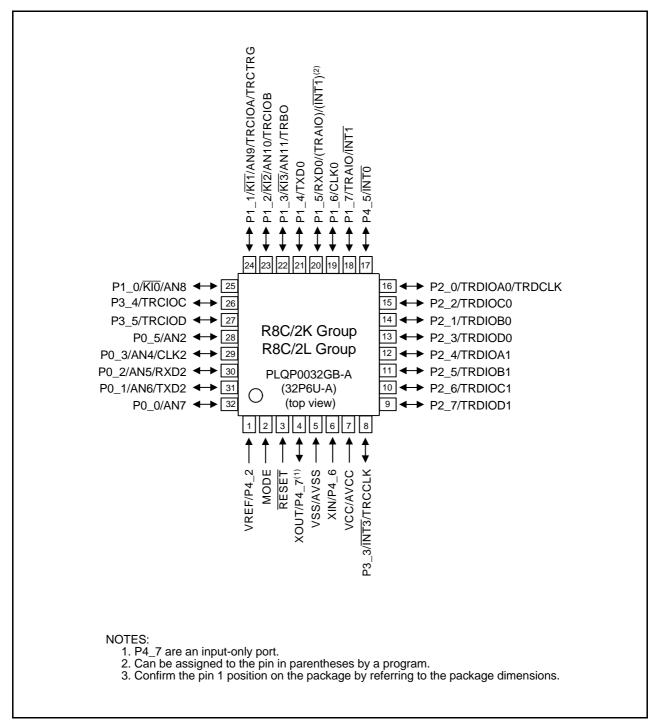


Figure 1.4 Pin Assignment (Top View)

Table 1.7 Pin Name Information by Pin Number

Pin Control Pin Port		Dort	I/O Pin Functions for of Peripheral Modules			
Number	Control Pili	Polt	Interrupt	Timer	Serial Interface	A/D Converter
1	VREF	P4_2				
2	MODE					
3	RESET					
4	XOUT	P4_7				
5	VSS/AVSS					
6	XIN	P4_6				
7	VCC/AVCC					
8		P3_3	ĪNT3	TRCCLK		
9		P2_7		TRDIOD1		
10		P2_6		TRDIOC1		
11		P2_5		TRDIOB1		
12		P2_4		TRDIOA1		
13		P2_3		TRDIOD0		
14		P2_1		TRDIOB0		
15		P2_2		TRDIOC0		
16		P2_0		TRDIOA0/TRDCLK		
17		P4_5	ĪNT0			
18		P1_7	INT1	TRAIO		
19		P1_6			CLK0	
20		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0	
21		P1_4			TXD0	
22		P1_3	KI3	TRBO		AN11
23		P1_2	KI2	TRCIOB		AN10
24		P1_1	KI1	TRCIOA/TRCTRG		AN9
25		P1_0	KI0			AN8
26		P3_4		TRCIOC		
27		P3_5		TRCIOD		
28		P0_5				AN2
29		P0_3			CLK2	AN4
30		P0_2			RXD2	AN5
31		P0_1			TXD2	AN6
32		P0_0				AN7

1. Can be assigned to the pin in parentheses by a program.

1.5 Pin Functions

Table 1.8 lists Pin Functions.

Table 1.8 Pin Functions

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	_	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	-	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between
XIN clock output	XOUT	0	the XIN and XOUT pins ⁽¹⁾ . To use an external clock, input it to the XIN pin and leave the XOUT pin open.
INT interrupt input	ĪNTO, ĪNT1, ĪNT3	I	INT interrupt input pins. INT0 is timer RB, timer RC and timer RD input pins.
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
Timer RB	TRBO	0	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Serial interface	CLK0, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD2	I	Serial data input pins
	TXD0, TXD2	0	Serial data output pins
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN2, AN4 to AN11	I	Analog input pins to A/D converter
I/O port	P0_0 to P0_3, P0_5, P1_0 to P1_7, P2_0 to P2_7, P3_3 to P3_5, P4_5,	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input

O: Output

I/O: Input and output

NOTE:

1. Refer to the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

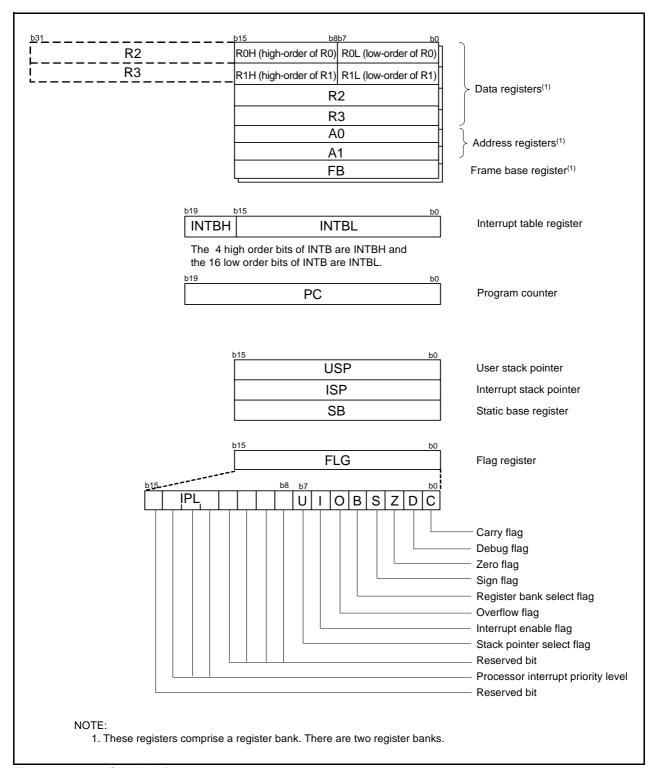


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 **Interrupt Table Register (INTB)**

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 **Program Counter (PC)**

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.



2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. **Memory**

3.1 **R8C/2K Group**

Figure 3.1 is a Memory Map of R8C/2K Group. The R8C/2K Group has 1 Mbyte of address space from addresses

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1.5-Kbyte internal RAM area is allocated addresses 00400h to 009FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

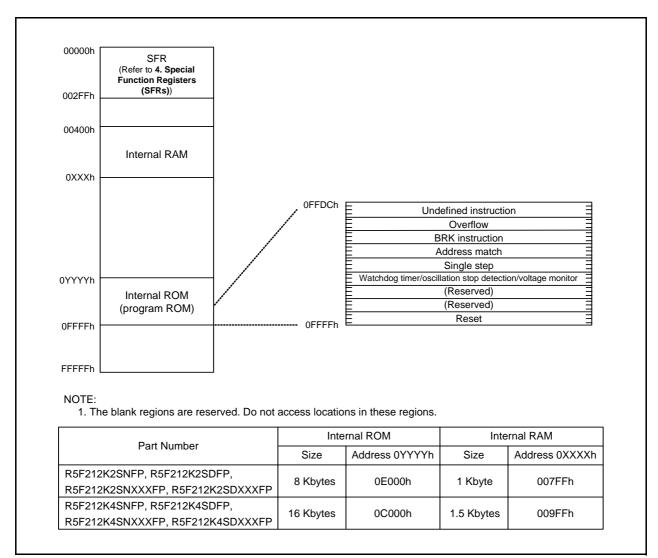


Figure 3.1 Memory Map of R8C/2K Group

3.2 R8C/2L Group

Figure 3.2 is a Memory Map of R8C/2L Group. The R8C/2L Group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 1.5-Kbyte internal RAM is allocated addresses 00400h to 009FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

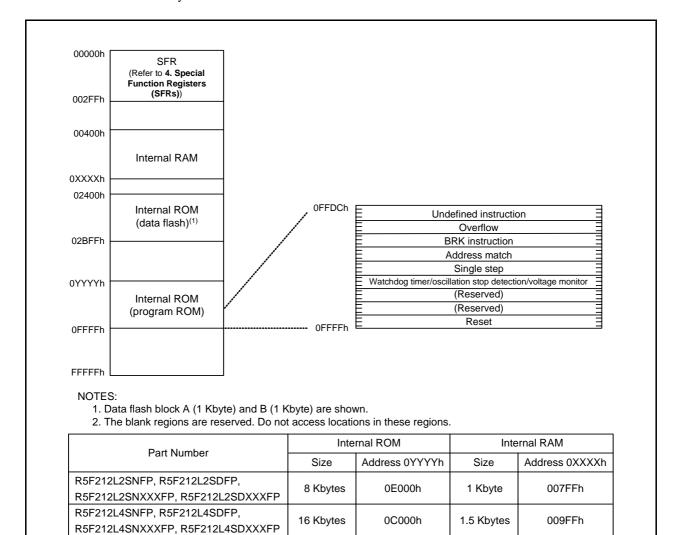


Figure 3.2 Memory Map of R8C/2L Group

Special Function Registers (SFRs) 4.

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

SFR Information (1)⁽¹⁾ Table 4.1

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h 0004h	December Made Parieta 0	DMO	001-
	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1 System Clock Control Register 0	PM1 CM0	00h
0006h			01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h 0009h			
0009h	Drotost Dogistor	PRCR	00h
000An	Protect Register	PRCR	oon
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Ch	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000En	Watchdog Timer Staft Register Watchdog Timer Control Register	WDC	00X11111b
000Fn	Address Match Interrupt Register 0	RMAD0	00X11111b
0010H	Address Match Interrupt Register 0	RIVIADO	00h
001111 0012h	4		00h
0012h 0013h	Address Match Interrupt Enable Register	AIER	00h
0013h	Address Match Interrupt Enable Register Address Match Interrupt Register 1	RMAD1	00h
0014h	Address Match Interrupt Negister 1	KIVIADI	00h
0015h	4		00h
0016H			0011
0017h			
0019h			
0013h			
001An			
001Ch	Count Source Protection Mode Register	CSPR	00h
001011	Count Course 1 Totalion Would Register	00110	10000000b ⁽⁶⁾
001Dh			10000000b(=)
001Eh			
001En			
001111 0020h			
002011 0021h			
002111 0022h			
0022h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0023h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0024h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	Thigh opeca on only oscillator control register 2	11002	0011
0027h			
0028h			
0020h			
0023h			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When Shipping
	1 3 -1 -1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -	1	1
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 1(2)	VCA2	00h ⁽³⁾
000 <u>L</u> II	Vollage Detection (Vegister 20)	V 0, 12	00100000b ⁽⁴⁾
0033h			00100000000
0033h 0034h			
0035h 0036h	Voltage Manitor 4 Circuit Control Danieta (5)	VW1C	00001000b
0036h	Voltage Monitor 1 Circuit Control Register(5)	VW1C	00001000b
	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾		
0038h	Voltage Monitor 0 Circuit Control Register ⁽²⁾	VW0C	0000X000b ⁽³⁾
			0100X001b ⁽⁴⁾
0039h			
003Ah			
			· · · · · · · · · · · · · · · · · · ·
003Eh 003Fh			

X: Undefined

- The blank regions are reserved. Do not access locations in these regions.

 Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.

 The LVD0ON bit in the OFS register is set to 1 and hardware reset.

- Power-on reset, voltage monitor 0 reset, or the LVDOON bit in the OFS register is set to 0 and hardware reset. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3. The CSPROINI bit in the OFS register is set to 0.

SFR Information (2)⁽¹⁾ Table 4.2

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah			
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Eh	77D CONVERSION INTERPRETATION REGISTER	7.BIO	7000000000
0050h		+	
0050H	UART0 Transmit Interrupt Control Register	SOTIC	XXXXX000b
0051h	UARTO Transmit interrupt Control Register	SORIC	XXXXX000b
0052H	Oractio receive interrupt Control register	SUNIC	AAAAA000D
0053h			
0055h			
0056h	Timor PA Interrupt Control Pogister	TRAIC	XXXXX000b
	Timer RA Interrupt Control Register	TRAIC	AAAAAUUD
0057h	Times DD Intervent Control Degister	TDDIO	VVVVVOCCE
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah		1	
006Bh		1	
006Ch		1	
006Dh			
006Eh		1	
006Fh			
0070h		<u> </u>	<u> </u>
0071h		<u> </u>	<u> </u>
0071h		+	
0072h		+	
0074h		-	
0075h			-
0075h		+	+
0077h		+	+
007711 0078h			
0078h			
0079h			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh	1	1	1

X: Undefined
NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

SFR Information (3)⁽¹⁾ Table 4.3

Address	Register	Symbol	After reset
0080h	rtegister	Gymbol	Aitel Teset
0081h			
0081H			
0082h			
0084h			
0085h			
0086h			
0087h 0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
		0010	70/01
00A3h		0016	XXh
00A3h 00A4h	UART0 Transmit/Receive Control Register 0	U0C0	XXh 00001000b
00A3h 00A4h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1		XXh 00001000b 00000010b
00A3h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h	UART0 Transmit/Receive Control Register 0	U0C0 U0C1	XXh 00001000b 00000010b
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ADh	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ADh	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ADh 00AEh 00AFh	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ADh 00AEh 00AEh	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ADh 00AEh 00AEh 00B1h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ADh 00AFh 00B0h 00B1h 00B2h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ACh 00ACh 00ACh 00AFh 00B1h 00B2h 00B3h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A6h 00A7h 00A8h 00A9h 00AAh 00ACh 00ACh 00ACh 00B1h 00B2h 00B2h 00B3h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ACh 00ACh 00AFh 00B6h 00B1h 00B2h 00B3h 00B4h 00B5h 00B6h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ACh 00ACh 00AEh 00B1h 00B2h 00B3h 00B4h 00B5h 00B6h 00B7h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ACh 00ACh 00B1h 00B2h 00B3h 00B4h 00B5h 00B6h 00B7h 00B8h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ACh 00ACh 00AFh 00B6h 00B1h 00B2h 00B3h 00B4h 00B5h 00B6h 00B7h 00B8h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ACh 00ACh 00ACh 00ACh 00B1h 00B2h 00B3h 00B4h 00B5h 00B6h 00B7h 00B6h 00B7h 00B8h 00B9h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ACh 00ACh 00ACh 00B1h 00B2h 00B3h 00B4h 00B5h 00B6h 00B7h 00B8h 00B8h 00B8h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ACh 00ACh 00B1h 00B1h 00B3h 00B4h 00B5h 00B6h 00B7h 00B8h 00B8h 00B8h 00BAh 00BBh	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A4h 00A5h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ACh 00ACh 00B1h 00B2h 00B3h 00B4h 00B5h 00B6h 00B7h 00B8h 00B9h 00BAh 00BAh 00BAh	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh
00A3h 00A4h 00A5h 00A6h 00A6h 00A7h 00A8h 00A9h 00AAh 00ABh 00ACh 00ACh 00ACh 00B1h 00B2h 00B3h 00B5h 00B6h 00B7h 00B8h 00B8h 00B8h 00B8h 00B8h 00B8h	UART0 Transmit/Receive Control Register 0 UART0 Transmit/Receive Control Register 1	U0C0 U0C1	XXh 00001000b 00000010b XXh

X: Undefined
NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

SFR Information (4)⁽¹⁾ Table 4.4

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h	<u>] </u>		XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D111	+		+
00D2H			+
00D3H	A/D Control Register 2	ADCON2	00h
00D4h	A/D CONTROL Negister 2	ADCONZ	0011
00D5fi	A/D Control Register 0	ADCON0	00h
00D6h	A/D Control Register 0 A/D Control Register 1	ADCON0 ADCON1	00h
00D7h	A/D Control Megister 1	ADCONT	0011
00D8h			
00DAh 00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh	, i		
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P2 Drive Capacity Control Register	P2DRR	00h
00F4H	Pin Select Register 1	PINSR1	XXh
00F6h	Pin Select Register 2	PINSR2	XXh
00F6fi	Pin Select Register 3	PINSR2 PINSR3	XXh
	Port Mode Register		
00F8h		PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX000000b
00FEh 00FFh			

X: Undefined
NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

SFR Information (5)⁽¹⁾ Table 4.5

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0100h	Timer RA I/O Control Register	TRAIOC	00h
0101h	Timer RA Mode Register	TRAMR	00h
0102H	Timer RA Prescaler Register	TRAPRE	FFh
0103H	Timer RA Register	TRA	FFh
0104H	LIN Control Register 2	LINCR2	00h
0105h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h	 		<u> </u>
0114h	 		
0115h	+		+
0116h	+		
0116H			+
0117H			
0119h			
1			
011Ah			
011Bh			
011Ch			
011Dh			
011Eh			
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h	1	1	00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h	Timor No Conordi Register 71		
012311		TROOKA	
012Δh	Timer RC General Register B		FFh
012Ah 012Bh	Timer RC General Register B	TRCGRB	FFh FFh
012Bh	1	TRCGRB	FFh FFh FFh
012Bh 012Ch	Timer RC General Register B Timer RC General Register C		FFh FFh FFh FFh
012Bh 012Ch 012Dh	Timer RC General Register C	TRCGRB	FFh FFh FFh FFh FFh
012Bh 012Ch 012Dh 012Eh	1	TRCGRB	FFh FFh FFh FFh FFh FFh
012Bh 012Ch 012Dh 012Eh 012Fh	Timer RC General Register C Timer RC General Register D	TRCGRB TRCGRC TRCGRD	FFh FFh FFh FFh FFh FFh
012Bh 012Ch 012Dh 012Eh 012Fh 0130h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2	TRCGRB TRCGRC TRCGRD TRCCR2	FFh FFh FFh FFh FFh FFh O0011111b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh FFh O0011111b 00h
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2	TRCGRB TRCGRC TRCGRD TRCCR2	FFh FFh FFh FFh FFh FFh O0011111b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh FFh O0011111b 00h
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh FFh O0011111b 00h
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh FFh O0011111b 00h
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh FFh O0011111b O0h 01111111b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register Timer RD Start Register	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF TRCOER TRCOER	FFh FFh FFh FFh FFh O0011111b 00h 01111111b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register Timer RD Start Register Timer RD Mode Register	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF TRCOER TRDSTR TRDMR	FFh FFh FFh FFh FFh O0011111b 00h 01111111b
012Bh 012Ch 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register Timer RD Start Register Timer RD Mode Register Timer RD PWM Mode Register	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF TRCOER TRDSTR TRDMR TRDPMR	FFh FFh FFh FFh FFh FON FFN FFN FFN FON FON FON FON FON FON
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register Timer RD Start Register Timer RD Mode Register	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF TRCOER TRDSTR TRDMR	FFh FFh FFh FFh FFh O0011111b 00h 01111111b
012Bh 012Ch 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register Timer RD Start Register Timer RD Mode Register Timer RD PWM Mode Register Timer RD Function Control Register Timer RD Output Master Enable Register	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF TRCOER TRDSTR TRDMR TRDPMR	FFh FFh FFh FFh FFh FON FFN FFN FFN FON FON FON FON FON FON
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h 0138h 0139h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register Timer RD Start Register Timer RD Mode Register Timer RD PWM Mode Register Timer RD Function Control Register Timer RD Output Master Enable Register	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF TRCOER TRDSTR TRDMR TRDPMR TRDPMR TRDFCR	FFh FFh FFh FFh FFh FFh O0011111b O0h 01111111b 11111100b 00001110b 10001000
012Bh 012Ch 012Dh 012Eh 012Fh 0136h 0131h 0132h 0133h 0134h 0135h 0136h 0137h 0138h 0139h 0139h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register Timer RD Output Master Enable Register Timer RD Mode Register Timer RD PWM Mode Register Timer RD Function Control Register Timer RD Output Master Enable Register 1 Timer RD Output Master Enable Register 2	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF TRCOER TRDSTR TRDMR TRDPMR TRDFCR TRDFCR TRDOER1 TRDOER2	FFh FFh FFh FFh FFh FFh O0011111b O0h 01111111b 11111100b 00001110b 10001000
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h 0138h 0139h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register Timer RD Start Register Timer RD Mode Register Timer RD PWM Mode Register Timer RD Function Control Register Timer RD Output Master Enable Register	TRCGRB TRCGRC TRCGRD TRCCR2 TRCDF TRCOER TRDSTR TRDMR TRDPMR TRDPMR TRDFCR TRDOER1	FFh FFh FFh FFh FFh FFh O0011111b O0h 01111111b 11111100b 00001110b 10001000

NOTE:

1. The blank regions are reserved. Do not access locations in these regions

SFR Information (6)⁽¹⁾ Table 4.6

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h	UART2 Transmit/Receive Mode Register	U2MR	00h
0161h	UART2 Bit Rate Register	U2BRG	XXh
0162h	UART2 Transmit Buffer Register	U2TB	XXh
0163h			XXh
0164h	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
0165h	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
0166h	UART2 Receive Buffer Register	U2RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
	1		
017Eh 017Fh			

X: Undefined NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

SFR Information (7)⁽¹⁾ Table 4.7

0180h 0182h 0182h 0182h 0182h 0183h 0183h 0188h 018h 01	Address	Register	Symbol	After reset
0181h	0180h	rogistor	Cymbol	71101 10001
0183h 0183h 0186h 0186h 0186h 0187h 0187h 0188h 0186h 0196h	0181h			
0183h 0183h 0186h 0186h 0186h 0187h 0187h 0188h 0186h 0196h				
0186h 0187h 0188h 0198h 0199h 0199h 0199h 0199h 0199h 0199h 0199h 0199h 0199h 0198h	0183h			
0188h	0184h			
0187h 0188h				
0189h 018An 018An 018An 018An 018Ch 018Ch 018Ch 018Ch 018Ch 018Eh 018Ch 018Eh 019Ch 019Ch 019Ch 019Sh 01ASh	0186h			
0188h 0188h 0188h 0188h 0188h 018b 018ch 019ch 0	0187h			
018Ah 018Ch 018Ch 018Ch 018Eh 018Eh 018Eh 019M 019M 019M 019M 019M 019M 019M 019M	0188h			
018Bh 018Ch 018Ch 018Ch 018Eh 018Fh 019Ph 0190h 0191h 0193h 0193h 0198h 0143h 0143h 0143h 0144h 0142h 0143h 0148h 0158h 0158h 0158h	0189h			
018Ch	018Ah			
018Dh 018Ph 018Ph 0190h 0191h 0191h 0192h 0193h 0194h 0196h 0197h 0198h 014Ah	018Bh			
018Eh 0199h 0199h 0192h 0192h 0192h 0193h 0194h 0198h 0197ch 017A2h 017A2h 017A3h 017A4h 017A2h 017A3h 017A4h 017A5h 017A6h 017A7h 017A8h	018Ch			
018Fh 0191h 0191h 0192h 0192h 0193h 0194h 0195h 0195h 0196h 0197h 0198h 0199h 0199h 0190h 0190h 0191h 0190h 0192h 0190h 0192h 0190h 0192h 0140h 0140h 0141h 0142h 0144h 0142h 0143h 0144h 0144h 0145h 0147h 0148h 0147h 0148h 0148h 0185h Flash Memory Control Register 4 FMR1 0186h 0186h 0186h 0188h 0198h 0198h 0188h 0198h <t< td=""><td></td><td></td><td></td><td></td></t<>				
0190h 0192h 0192h 0192h 0193h 0194h 0195h 0196h 0197h 0198h 0198h 0199h 0198h 0199h 0192h 0192h 0142h 0142h 0142h <td>010EII</td> <td></td> <td></td> <td></td>	010EII			
0191h 0193h 0193h 0193h 0194h 0195h 0195h 0195h 0197h 0197h 0198h 0199h 0199h 0199h 019Ch 019Dh 019Eh 019Fh 014Ah 014Ah 014Bh 014Ah 014Bh 014Ah 014Bh 014Ah 014Bh 014Bh 014Bh 014Bh 014Bh 016Bh 01Bh 016Bh 01Bh 016Bh 01Bh				
0192h 0194h 0194h 0195h 0196h 0197h 0197h 0198h 0199h 0199h 0191h 0191h 0192h 0192h 014th 0192h 014th 014th 014th <td></td> <td></td> <td></td> <td></td>				
0193h 0195h 0195h 0196h 0197h 0197h 0198h 0199h 0199h 0199h 019Dh 019Dh 019Eh 019Dh 019Fh 019Fh 01A3h 0141h 01A3h 01A3h 01A3h 01A3h 01A3h 01A3h 01A3h 01A4h 01A7h 01A8h 01A8h 01A8h 01A8h 01A8h 01ABh 01ABh 01ACh 01ABh 01APh 01Bh 01Bh 01Bh	0192h			
0194h 0196h 0197h 0188h 0197h 0198h 0199h 0199h 0190h 0198h 0190h 0198h 0190h 0199h 0190h 0199h 0190h 0199h 0190h 0199h 0191h 0199h 0192h 0199h 0197h 0100 0140h 0140h 0141h 0140h 0142h 0143h 0144h 0148h 0148h 0148h 015h 018h 018h 0	0193h			
0195h 0197h 0197h 0198h 0199h 0199h 0199h 0199h 0190h 019Dh 019Dh 019Eh 019Eh 013Eh 01Alh	0194h			
0196h 0198h 0199h 0199h 0199h 0199h 0198h 0190h 0190h 0190h 0190h 0190h 0190h 0190h 0190h 0190h 0100h	0195h			
0198h	0196h			
0199h				
019Ah 019Bh 019Ch 019Dh 019Eh 019Fh 019Fh 01A0h 01A1h 01A2h 01A2h 01A3h 01A3h 01A8h 01A6h 01A8h 01A8h 01A8h 01A8h 01A8h 01AAh 01A8h 01ACh 01ACh 01ACh 01ACh 01ACh 01ACh 01ACh 01ACh 01AEh 01ACh 01AEh 01BCh 01Bith 01Bith				
019Bh 019Dh 019Ch 019Bh 019Fh 019Fh 01A0h 01A1h 01A1h 01A2h 01A3h 01A3h 01A6h 01A6h 01A8h 01A8h 01A8h 01A8h 01A8h 01A8h 01A8h 01A8h 01ABh 01ABh 01ACh 01ABh 01ACh 01ABh 01ABh 01ABh 01Bh 01Bh 01Bh 01Bh 01Bh 01Bh 01Bh 10Bh 01Bh 10Bh <td></td> <td></td> <td></td> <td></td>				
019Ch 019Eh 019Eh 019Eh 019Fh 01000 01A0h 01A1h 01A2h 01A3h 01A3h 01A3h 01A6h 01A7h 01A8h 01A7h 01A8h 01A8h 01AAh 01A8h 01AAh 01ABh 01ACh 01ACh 01ACh 01ACh 01ABh 01ACh 01ABh 01ACh 01ABh 01ACh 01Bh 01Bh 01Bh 01Bh 01Bh 01Bh 01Bh 01Bh 01Bh 1Bh 01Bh Flash Memory Control Register 1 01Bh 1Bh 01Bh 01Bh 01Bh				
019Ch	019Bh			
019Eh	019Ch			
019Fh	019Dh			
0140h 0142h 0142h 0143h 0143h 0144h 0145h 0146h 0147h 0148h 0148h 0148h 0148h 0148h 0148h 0148h 0148h 0148h 0158h 0168h 0168h 0187h 0188h	019En			
0142h 0142h 0143h 0144h 0145h 0146h 0146h 0147h 0148h 0158h 0168h 0168h 0189h 0188h				
01A2h 01A3h 01A4h 01A5h 01A5h 01A7h 01A8h 01A8h 01A9h 01A8h 01A8h 01ABh 01ABh 01ABh 01ABh 01ABh 01ABh 01Bh 01ABh 01Bh 01Bh 01Bh 01Bh 01Bh 01Bh 01Bh 01	01A011			
01A3h	01A111			
01A4h 01A5h 01A6h 01A7h 01A8h 01A9h 01AAh 01ABh 01ABh 01ACh 01ABh 01ABh 01ABh 01ABh 01ABh 01BBh	01A3h			
0145h 0146h 0147h 0148h 0149h 014Ah 014Ah 014Ah 014Ah 014Ah 014Ch 014ACh 014AFh 014Fh 018Dh 018Bh 018Bh Flash Memory Control Register 4 FMR4 018Bh 018Bh Flash Memory Control Register 1 FMR1 1000000Xb 01B7h Flash Memory Control Register 0 FMR0 01000001b 01B8h				
01A6h 01A7h 01A8h 01A8h 01A9h 01AAh 01ABh 01ABh 01ACh 01ADh 01AEh 01AEh 01AFh 01BDh 01B0h 01B1h 01B2h 01B3h 01B3h Flash Memory Control Register 4 01B5h Flash Memory Control Register 1 01B6h 01B6h 01B8h 01B9h 01B9h 01B9h 01BCh 01BCh 01BCh 01BCh 01BFh 01BEh 01BFh 01BEh	01A5h			
01A7h 01A8h 01A9h 01AAh 01ABh 01ACh 01ACh 01ACh 01AFh 01B1h 01B2h 01B2h 01B3h 01B4h 01B5h 01B5h Flash Memory Control Register 4 01B6h 01B7h Flash Memory Control Register 0 FMR0 01B9h 01B7h 01B8h 01B8h 01B8h 01B8h 01B9h 01B8h 01B9h 01B9h 01BBh 01BBh 01BBh 01BBCh 01BCh 01BCh 01BEh	01A6h			
01A9h 01AAh 01ABh 01ACh 01ACh 01AEh 01AFh 01B0h 01B1h 01B2h 01B3h Flash Memory Control Register 4 01B4h 01B5h Flash Memory Control Register 1 01B6h 01B7h Flash Memory Control Register 0 01B8h 01B9h 01BAh 01BCh 01BCh 01BFh				
01AAh 01ABh 01ACh 01ACh 01ADh 01AEh 01AFh 01B0h 01B0h 01B1h 01B2h 01B3h 01B3h Flash Memory Control Register 4 FMR4 01000000b 01B4h 01B5h Flash Memory Control Register 1 FMR1 1000000Xb 01B6h 01B7h Flash Memory Control Register 0 FMR0 00000001b 01B8h 01B9h 01BAh 01BBh 01BCh 01BCh 01BCh 01BCh 01BCh 01BFh 01BFh 01BFh 01BFh	01A8h			
01ABh 01ACh 01ADh 01ADh 01AEh 01AFh 01AFh 01B0h 01B0h 01B1h 01B2h 01B2h 01B3h Flash Memory Control Register 4 FMR4 01000000b 01B4h 01B5h Flash Memory Control Register 1 FMR1 1000000Xb 01B7h Flash Memory Control Register 0 FMR0 00000001b 01B8h 01B8h 01B8h 01B8h 01BBh 01BCh 01BCh 01BCh 01BCh 01BFh 01BFh 01BFh	01A9h			
01ACh 01ADh 01AEh 01AFh 01B0h 01B0h 01B1h 01B2h 01B3h Flash Memory Control Register 4 FMR4 010000000b 01B4h 01B5h Flash Memory Control Register 1 FMR1 1000000Xb 01B6h 01B7h Flash Memory Control Register 0 FMR0 00000001b 01B8h 01B9h 01BAh 01BBh 01BCh 01BCh 01BCh 01BCh 01BFh 01BFh 01BFh 01BFh	01AAh			
01ADh 01AEh 01AFh 01B0h 01B1h 01B2h 01B3h Flash Memory Control Register 4 FMR4 01B4h 01B5h Flash Memory Control Register 1 FMR1 01B6h 01B7h Flash Memory Control Register 0 FMR0 01B8h 01B8h 01BBh 01BCh 01BFh 01BFh	01ABh			
01AEh 01AFh 01B0h 01B1h 01B2h 01B2h 01B3h Flash Memory Control Register 4 FMR4 010000000b 01B4h 01B5h FMR1 1000000Xb 01B6h FMR1 1000000Xb 01B7h Flash Memory Control Register 0 FMR0 00000001b 01B8h 01B8h 01BAh 01BAh 01BCh 01BCh 01BCh 01BCh 01BFh 01BFh 01BFh 01BFh	01ACh			
01AFh 01B0h 01B1h 01B1h 01B2h 01B2h 01B3h Flash Memory Control Register 4 FMR4 010000000b 010000000b 010000000b 010000000b 010000000b 0100000000b 0100000000b 0100000000b 0100000000b 0100000000b 0100000000b 0100000000b 010000000000b 0100000000b 0100000000b 0100000000b 0100000000b 0100000000b 0100000000b 010000000b 0100000000b 0100000000b 0100000000b 010000000b 0100000000b 010000000b 01000000b 0100000b 0100000b 0100000b 0100000b 01000000b 01000000b 0100000b 0100000b <t< td=""><td></td><td></td><td></td><td></td></t<>				
01B0h 01B1h 01B2h 01B3h 01B3h Flash Memory Control Register 4 FMR4 01000000b 01B4h 01B5h Flash Memory Control Register 1 FMR1 10000000xb 01B6h 01B7h Flash Memory Control Register 0 FMR0 00000001b 01B8h 01B9h 01B9h 01B9h 01B9h 01BBh 01BCh 01BCh 01BCh 01BCh 01BCh 01BFh 01BFh <td></td> <td></td> <td></td> <td></td>				
01B1h 01B2h 01B3h Flash Memory Control Register 4 FMR4 01000000b 01B4h 01B5h Flash Memory Control Register 1 FMR1 10000000xb 01B6h 01B7h Flash Memory Control Register 0 FMR0 00000001b 01B8h 0 01B9h 00000001b 01BAh 0 00000001b 01BBh 0 00000001b 01BCh 000000000000000000000000000000000000	01AFN			
01B2h 01B3h Flash Memory Control Register 4 FMR4 01000000b 01B4h 01B5h Flash Memory Control Register 1 FMR1 1000000Xb 01B6h 01B7h Flash Memory Control Register 0 FMR0 00000001b 01B8h 01B9h 01B9h 01BBh 01BBh 01BBh 01BCh 01BCh 01BCh 01BBh 01BFh 01BFh 01BFh 01BFh	01B0H			
01B3h Flash Memory Control Register 4 FMR4 010000000b 01B4h 01B5h Flash Memory Control Register 1 FMR1 10000000xb 01B6h 01B7h Flash Memory Control Register 0 FMR0 00000001b 01B8h 01B9h 01B9h 01B9h 01B9h 01BBh 01BCh 01BDh 01BDh 01BBh 01BFh 01BFh 01BFh 01BFh 01BFh	01B1II			
01B4h 01B5h Flash Memory Control Register 1 FMR1 1000000Xb 01B6h 01B7h Flash Memory Control Register 0 FMR0 00000001b 01B8h 01B9h 01B9h 01B9h 01B9h 01BBh 01BCh		Flash Memory Control Register 4	FMR4	01000000b
01B5h Flash Memory Control Register 1 FMR1 1000000Xb 01B6h Flash Memory Control Register 0 FMR0 00000001b 01B8h 01B9h 01B9h 01B9h 01B9h 01BBh 01BCh 01BCh 01BDh 01BDh 01BFh 01BFh 01BFh 01BFh	01B4h			
01B6h 01B7h Flash Memory Control Register 0 FMR0 00000001b 01B8h 01B9h	01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B7h Flash Memory Control Register 0 FMR0 00000001b 01B8h 01B9h 01B4h 01B4h 01B6h <	01B6h			
01B8h 01B9h 01BAh 01BAh 01BBh 01BCh 01BCh 01BDh 01BEh 01BFh	01B7h	Flash Memory Control Register 0	FMR0	00000001b
01BAh 01BBh 01BCh 01BDh 01BDh 01BEh 01BFh	01B8h			
01BBh 01BCh 01BDh 01BEh 01BFh	01B9h			
01BCh 01BDh 01BEh 01BFh	01BAh			
01BDh 01BEh 01BFh	01BBh			
01BEh 01BFh	01BCh			
01BFh	01BDh			
	01BEh			
	UIBFh			
L ELEED LODGED Eurotion Soloot Pogistor LAST 1/Note 01	CCCCh	Option Function Select Register	I OES	(Note 2)
FFFFh Option Function Select Register OFS (Note 2)	FFFFN	Option Function Select Register	UFO	(NOTE 2)

X: Undefined
NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Electrical Characteristics

The electrical characteristics of N version (Topr = -20° C to 85° C) and D version (Topr = -40° C to 85° C) are listed below.

Please contact Renesas Technology sales offices for the electrical characteristics in the Y version (Topr = -20° C to 105° C).

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
Vcc/AVcc	Supply voltage		-0.3 to 6.5	V
Vı	Input voltage		-0.3 to Vcc + 0.3	V
Vo	Output voltage		-0.3 to Vcc + 0.3	V
Pd	Power dissipation	Topr = 25°C	500	mW
Topr	Operating ambient temperature		-20 to 85 (N version) / -40 to 85 (D version)	°C
Tstg	Storage temperature		-65 to 150	°C

Recommended Operating Conditions Table 5.2

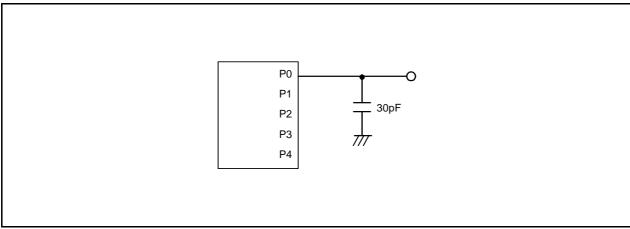
Symbol	Parameter		Conditions		Standard		Unit
Symbol	'	rafametei	Conditions	Min.	Тур.	Max.	Oill
Vcc	Supply voltage			2.2	-	5.5	V
AVcc	Supply voltage			2.7	-	5.5	
Vss/AVss	Supply voltage			-	0	-	V
VIH	Input "H" voltage			0.8 Vcc	_	Vcc	V
VIL	Input "L" voltage			0	_	0.2 Vcc	V
IOH(sum)	Peak sum output "H" current	Sum of all pins IOH(peak)		=	=	-160	mA
IOH(sum)	Average sum output "H" current	Sum of all pins IOH(avg)		-	_	-80	mA
IOH(peak)	Peak output "H"	Except P2_0 to P2_7		_	_	-10	mA
	current	P2_0 to P2_7		-	-	-40	mA
IOH(avg)	Average output	Except P2_0 to P2_7		-	-	-5	mA
	"H" current	P2_0 to P2_7		_	=	-20	mA
IOL(sum)	Peak sum output "L" currents	Sum of all pins IOL(peak)		-	-	160	mA
IOL(sum)	Average sum output "L" currents	Sum of all pins IOL(avg)		-	-	80	mA
IOL(peak)	Peak output "L"	Except P2_0 to P2_7		-	-	10	mA
	currents	P2_0 to P2_7		-	=	40	mA
IOL(avg)	Average output	Except P2_0 to P2_7		-	=	5	mA
	"L" current	P2_0 to P2_7		-	=	20	mA
f(XIN)	XIN clock input osc	cillation frequency	3.0 V ≤ Vcc ≤ 5.5 V	0	_	20	MHz
	·		2.7 V ≤ Vcc < 3.0 V	0	-	10	MHz
			2.2 V ≤ Vcc < 2.7 V	0	=	5	MHz
_	System clock	OCD2 = 0	3.0 V ≤ Vcc ≤ 5.5 V	0	=	20	MHz
		XIN clock selected	2.7 V ≤ Vcc < 3.0 V	0	=	10	MHz
			2.2 V ≤ Vcc < 2.7 V	0	=	5	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	-	125	=	kHz
		SSIGGE	FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ Vcc ≤ 5.5 V	_	-	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ Vcc ≤ 5.5 V	_	-	10	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ Vcc ≤ 5.5 V	_	=	5	MHz

Vcc = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
 The average output current indicates the average value of current measured during 100 ms.

verter Characteristics
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Symbol		Parameter	Conditions	Standard			Unit
Symbol	'	raiametei	Conditions	Min.	Тур.	Max.	Offic
=	Resolution		Vref = AVCC	-	-	10	Bits
=	Absolute	10-bit mode	φAD = 10 MHz, Vref = AVCC = 5.0 V	=	-	±3	LSB
	accuracy	8-bit mode	φAD = 10 MHz, Vref = AVCC = 5.0 V	_	_	±2	LSB
		10-bit mode	φAD = 10 MHz, Vref = AVCC = 3.3 V	_	_	±5	LSB
		8-bit mode	φAD = 10 MHz, Vref = AVCC = 3.3 V	_	_	±2	LSB
Rladder	Resistor ladder		Vref = AVCC	10	_	40	kΩ
tconv	Conversion time	10-bit mode	φAD = 10 MHz, Vref = AVCC = 5.0 V	3.3	_	_	μS
		8-bit mode	φAD = 10 MHz, Vref = AVCC = 5.0 V	2.8	_	_	μS
Vref	Reference voltag	e		2.2	_	AVcc	V
VIA	Analog input volta	age ⁽²⁾		0	-	AVcc	V
_	A/D operating	Without sample and hold	Vref = AVCC = 2.7 to 5.5 V	0.25	_	10	MHz
	clock frequency	With sample and hold	Vref = AVCC = 2.7 to 5.5 V	1	-	10	MHz

- AVcc = 2.7 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
 When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.



Ports P0 to P4 Timing Measurement Circuit Figure 5.1

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Cymbal	Parameter	Conditions		Lloit		
Symbol	Parameter	Conditions	Min.	Тур.	- 400 9 97+CPU clock × 6 cycles 3+CPU clock × 4 cycles	Unit
_	Program/erase endurance ⁽²⁾	R8C/2K Group	100 ⁽³⁾	=	=	times
		R8C/2L Group	1,000(3)	-	-	times
=	Byte program time		=	50	400	μS
_	Block erase time		=	0.4	9	S
td(SR-SUS)	Time delay from suspend request until suspend		-	-		μS
_	Interval from erase start/restart until following suspend request		650	-	-	μS
_	Interval from program start/restart until following suspend request		0	-	-	ns
=	Time from suspend until program/erase restart		=	-		μS
_	Program, erase voltage		2.7	_	5.5	V
-	Read voltage		2.2	-	5.5	V
-	Program, erase temperature		0	-	60	°C
=	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	=	-	year

- NOTES:

 1. Vcc = 2.7 to 5.5 V at Topr = 0 to 60°C, unless otherwise specified.
 - 2. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions		Unit		
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
_	Program/erase endurance ⁽²⁾		10,000(3)	-	-	times
_	Byte program time (program/erase endurance ≤ 1,000 times)		_	50	400	μS
_	Byte program time (program/erase endurance > 1,000 times)		_	65	_	μS
_	Block erase time (program/erase endurance ≤ 1,000 times)		_	0.2	9	S
_	Block erase time (program/erase endurance > 1,000 times)		_	0.3	-	S
td(SR-SUS)	Time delay from suspend request until suspend		=	-	97+CPU clock × 6 cycles	μS
_	Interval from erase start/restart until following suspend request		650	-	_	μS
_	Interval from program start/restart until following suspend request		0	-	-	ns
_	Time from suspend until program/erase restart		_	-	3+CPU clock × 4 cycles	μS
-	Program, erase voltage		2.7	_	5.5	V
_	Read voltage		2.2	_	5.5	V
=	Program, erase temperature		-20 ⁽⁸⁾	-	85	°C
_	Data hold time ⁽⁹⁾	Ambient temperature = 55 °C	20	_	-	year

- 1. Vcc = 2.7 to 5.5 V at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
- 5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- 6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 8. -40°C for D version.
- 9. The data hold time includes time that the power supply is off or the clock is not supplied.

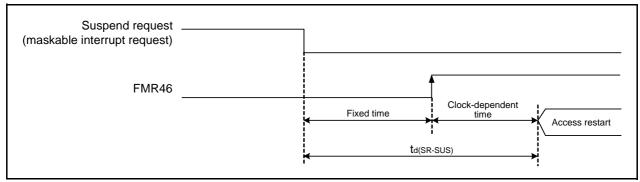


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vdet0	Voltage detection level		2.2	2.3	2.4	V
-	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	-	0.9	-	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		=	=	300	μS
Vccmin	MCU operating voltage minimum value		2.2	=	=	V

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version).
- 2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Syllibol	Faranietei	Condition	Min.	Тур.	Max.	Offic
Vdet1	Voltage detection level ⁽⁴⁾		2.70	2.85	3.00	V
=	Voltage monitor 1 interrupt request generation time ⁽²⁾		-	40	_	μS
=	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	=	0.6	=	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		-	-	100	μS

NOTES:

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
- 2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
- 3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
- 4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vdet2	Voltage detection level		3.3	3.6	3.9	V
-	Voltage monitor 2 interrupt request generation time ⁽²⁾		_	40	_	μS
=	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	=	0.6	=	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		=	=	100	μ\$

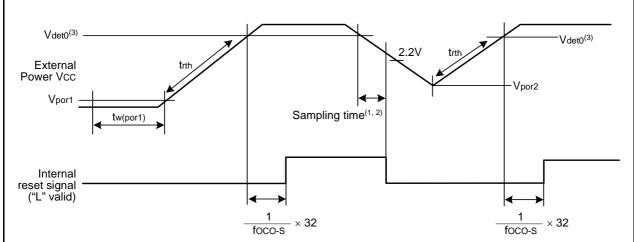
- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
- $2. \quad \text{Time until the voltage monitor 2 interrupt request is generated after the voltage passes $V_{\text{det}2}$.}$
- 3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.



Table 5.9	Power-on Reset Circuit.	Voltage Monitor 0 Reset Electrical Characteristics (3)
		Total go mornior o modern Endouncem on an action control

Symbol	Parameter	Condition		Unit		
Symbol	Faianetei	Condition	Min.	Тур.	Max.	Offic
Vpor1	Power-on reset valid voltage ⁽⁴⁾		_	-	0.1	V
Vpor2	Power-on reset or voltage monitor 0 reset valid voltage		0	_	Vdet0	V
trth	External power Vcc rise gradient(2)		20	_	_	mV/msec

- 1. The measurement condition is $T_{\text{opr}} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. This condition (external power Vcc rise gradient) does not apply if Vcc ≥ 1.0 V.
- 3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
- 4. tw(por1) indicates the duration the external power Vcc must be held below the effective voltage (Vpor1) to enable a power on reset. When turning on the power for the first time, maintain tw(por1) for 30 s or more if $-20^{\circ}\text{C} \le T_{opr} \le 85^{\circ}\text{C}$, maintain tw(por1) for 3,000 s or more if $-40^{\circ}\text{C} \le T_{opr} < -20^{\circ}\text{C}$.



- 1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
- 2. The sampling clock can be selected. Refer to 6. Voltage Detection Circuit for details.
- 3. Vdeto indicates the voltage detection level of the voltage detection 0 circuit. Refer to 6. Voltage Detection Circuit for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Cumbal	Doromotor	Condition		Unit		
Symbol	Parameter	Condition	Min.	Тур.	Max.	Offic
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	Vcc = 2.7 V to 5.5 V -20°C \le Topr \le 85°C ⁽²⁾	39.2	40	40.8	MHz
		Vcc = 2.7 V to 5.5 V -40° C \leq Topr \leq 85 $^{\circ}$ C ⁽²⁾	39.0	40	41.0	MHz
		Vcc = 2.2 V to 5.5 V -20° C \leq Topr \leq 85 $^{\circ}$ C ⁽³⁾	35.2	40	44.8	MHz
		Vcc = 2.2 V to 5.5 V -40° C \leq Topr \leq 85 $^{\circ}$ C ⁽³⁾	34.0	40	46.0	MHz
	High-speed on-chip oscillator frequency when	Vcc = 5.0 V, Topr = 25°C	_	36.864	_	MHz
	correction value in FRA7 register is written to FRA1 register ⁽⁴⁾	Vcc = 2.7 V to 5.5 V -20°C ≤ Topr ≤ 85°C	-3%	=	3%	%
_	Value in FRA1 register after reset		08h	_	F7h	-
_	Oscillation frequency adjustment unit of high- speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	-	+0.3	-	MHz
_	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	_	10	100	μS
=	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	_	550	_	μΑ

- Vcc = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
 These standard values show when the FRA1 register value after reset is assumed.
- 3. These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.
- 4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
_	Oscillation stability time		-	10	100	μS
=	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	-	15	-	μΑ

NOTE:

1. Vcc = 2.2 to 5.5 V, $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	,	Unit		
Symbol	r alametel	Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	=	2000	μS
td(R-S)	STOP exit time ⁽³⁾		-	-	150	μS

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = 25°C.
- Waiting time until the internal power supply generation circuit stabilizes during power-on.
- 3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.13 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit	
Symbol	Pai	rameter	Condition	וונ	Min.	Тур.	Max.	Offic	
Vон	Output "H"	Except P2_0 to P2_7,	Iон = −5 mA		Vcc - 2.0	=	Vcc	V	
	voltage	XOUT	IOH = -200 μA		Vcc - 0.5	1	Vcc	V	
		P2_0 to P2_7	Drive capacity HIGH	Iон = -20 mA	Vcc - 2.0	_	Vcc	V	
			Drive capacity LOW	Iон = −5 mA	Vcc - 2.0	=	Vcc	V	
		XOUT	Drive capacity HIGH	Iон = −1 mA	Vcc - 2.0	=	Vcc	V	
			Drive capacity LOW	IoH = -500 μA	Vcc - 2.0	=	Vcc	V	
Vol	Output "L" voltage	Except P2_0 to P2_7,	IoL = 5 mA		=	=	2.0	V	
		XOUT	IoL = 200 μA		=	=	0.45	V	
		P2_0 to P2_7	Drive capacity HIGH	IoL = 20 mA	=	=	2.0	V	
			Drive capacity LOW	IoL = 5 mA	=	=	2.0	V	
		XOUT	Drive capacity HIGH	IoL = 1 mA	=	=	2.0	V	
			Drive capacity LOW	IOL = 500 μA	=	=	2.0	V	
VT+-VT-	Hysteresis	INTO, INT1, INT3, KIO, KI1, KI2, KI3, TRAIO, RXDO, RXD2, CLK0, CLK2			0.1	0.5	_	V	
		RESET			0.1	1.0	-	V	
Іін	Input "H" current		VI = 5 V, Vcc = 5 V		-	_	5.0	μΑ	
lıL	Input "L" current		VI = 0 V, Vcc = 5 V		=	=	-5.0	μΑ	
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5 V		30	50	167	kΩ	
RfXIN	Feedback resistance	XIN			-	1.0	_	ΜΩ	
VRAM	RAM hold voltage		During stop mode		1.8	1	-	V	

^{1.} Vcc = 4.2 to 5.5 V at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.14 Electrical Characteristics (2) [Vcc = 5 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Doromatar	Condition	Standard			11-2	
Symbol	Parameter	Condition			Тур.	Max.	Unit
cur (Vo	Power supply current (Vcc = 3.3 to 5.5 V)	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	10	17	mA
	output pins are open, other pins are Vss	en, other pins Low-speed on-chip oscillator on = 125 kHz	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz	-	9	15	mA
	are vee		-	6	-	mA	
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	5	-	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	4		mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	2.5		mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	4	=	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	2.5	_	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	-	130	300	μА

Table 5.15 Electrical Characteristics (3) [Vcc = 5 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Cumbal	Doromotor		Condition		Standard	d	Unit
Symbol	Parameter	Condition		Min.	Тур.	Max.	Unit
cc Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins	Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	25	75	μА	
	are Vss	Stop mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	23	60	μА
			XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	0.8	3.0	μА
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	1.2	-	μА

Timing Requirements

(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.16 XIN Input

Symbol	Parameter		Standard		
Symbol	Parameter	Min.	Max.	Unit	
tc(XIN)	XIN input cycle time	50	-	ns	
twh(xin)	XIN input "H" width	25	-	ns	
twl(xin)	XIN input "L" width	25	-	ns	

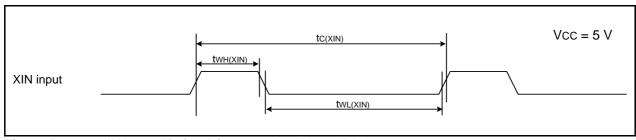


Figure 5.4 XIN Input Timing Diagram when Vcc = 5 V

Table 5.17 TRAIO Input

Symbol	Parameter -	Stan	Unit	
		Min.	Max.	Unit
tc(TRAIO)	TRAIO input cycle time	100	=	ns
tWH(TRAIO)	TRAIO input "H" width	40	=	ns
tWL(TRAIO)	TRAIO input "L" width	40	-	ns

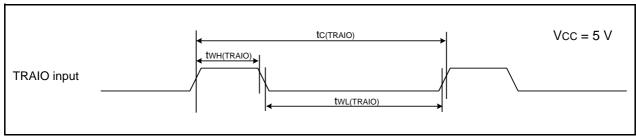


Figure 5.5 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.18 Serial Interface	Table	5.18	Serial	Interface
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Symbol	Parameter	Stan	Unit	
	Faidilletei	Min.	Max.	Offic
tc(CK)	CLKi input cycle time	200	-	ns
tW(CKH)	CLKi input "H" width	100	-	ns
tW(CKL)	CLKi input "L" width	100	-	ns
td(C-Q)	TXDi output delay time	-	50	ns
th(C-Q)	TXDi hold time	0	-	ns
tsu(D-C)	RXDi input setup time	50	=	ns
th(C-D)	RXDi input hold time	90	-	ns

i = 0, 2

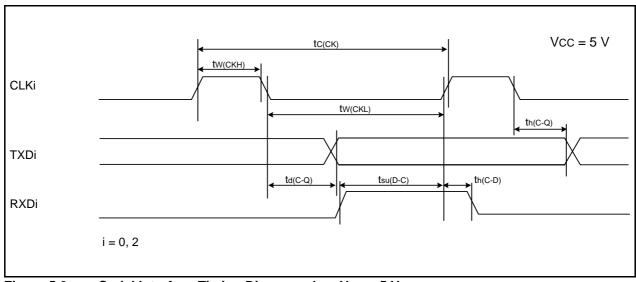


Figure 5.6 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.19 External Interrupt INTi (i = 0, 1, 3) Input

Symbol	Parameter	Stan	Unit	
Symbol	T diameter		Max.	Offic
tW(INH)	ĪNTi input "H" width	250 ⁽¹⁾	-	ns
tW(INL)	INTi input "L" width	250 ⁽²⁾	-	ns

NOTES:

- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

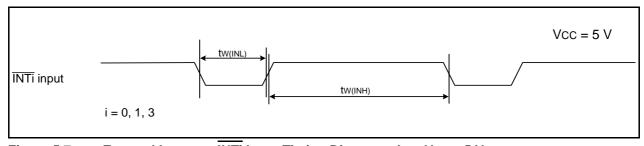


Figure 5.7 External Interrupt INTi Input Timing Diagram when Vcc = 5 V

Table 5.20 Electrical Characteristics (1) [Vcc = 3 V]

Symbol	Por	Parameter		Condition		Standard		
Symbol	Farameter Condition			Min.	Тур.	Max.	Unit	
Vон	Output "H" voltage	Except P2_0 to P2_7, XOUT	IOH = −1 mA		Vcc - 0.5	_	Vcc	V
		P2_0 to P2_7	Drive capacity HIGH	Iон = −5 mA	Vcc - 0.5	_	Vcc	V
			Drive capacity LOW	Iон = −1 mA	Vcc - 0.5	_	Vcc	V
		XOUT	Drive capacity HIGH	Iон = −0.1 mA	Vcc - 0.5	_	Vcc	V
			Drive capacity LOW	IOH = -50 μA	Vcc - 0.5	_	Vcc	V
Vol	Output "L" voltage	Except P2_0 to P2_7, XOUT	IoL = 1 mA	•	-	_	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	IOL = 5 mA	-	-	0.5	V
			Drive capacity LOW	IoL = 1 mA	-	_	0.5	V
		XOUT	Drive capacity HIGH	IOL = 0.1 mA	-	-	0.5	V
			Drive capacity LOW	IOL = 50 μA	-	_	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD2, CLK0, CLK2		•	0.1	0.3	-	V
		RESET			0.1	0.4	-	V
lін	Input "H" current	1	VI = 3 V, Vcc = 3	V	_	_	4.0	μΑ
lı∟	Input "L" current		VI = 0 V, Vcc = 3	V	-	-	-4.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V, $Vcc = 3$	V	66	160	500	kΩ
RfXIN	Feedback resistance	XIN			-	3.0	-	ΜΩ
VRAM	RAM hold voltage		During stop mode	e	1.8	_	_	V

NOTE:

^{1.} Vcc = 2.7 to 3.3 V at Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.21 Electrical Characteristics (2) [Vcc = 3 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Darameter		Condition		Standar	d	Unit
Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open,	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	6	_	mA
	other pins are Vss		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8		2	_	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	=	5	9	mA
		mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	=	2	-	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	-	130	300	μА
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	25	70	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	=	23	55	μА
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	0.7	3.0	μА
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	1.1	-	μА

Timing requirements

(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C) [Vcc = 3 V]

Table 5.22 XIN Input

Symbol	Parameter		Standard		
Symbol	Parameter	Min.	Max.	Unit	
tc(XIN)	XIN input cycle time	100	-	ns	
twh(xin)	XIN input "H" width	40	-	ns	
twl(xin)	XIN input "L" width	40	-	ns	

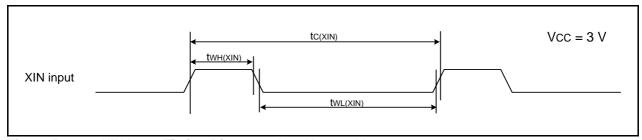


Figure 5.8 XIN Input Timing Diagram when Vcc = 3 V

Table 5.23 TRAIO Input

Symbol	Parameter		Standard		
	Parameter	Min.	Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	300	=	ns	
tWH(TRAIO)	TRAIO input "H" width	120	=	ns	
tWL(TRAIO)	TRAIO input "L" width	120	-	ns	

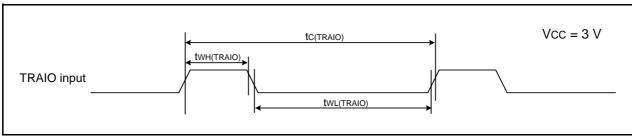


Figure 5.9 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.24 Serial Interface	Table	5.24	Serial	Interface
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Symbol	Parameter	Stan	Unit	
	raidilletei	Min.	Max.	Offic
tc(CK)	CLKi input cycle time	300	-	ns
tW(CKH)	CLKi input "H" width	150	-	ns
tW(CKL)	CLKi Input "L" width	150	-	ns
td(C-Q)	TXDi output delay time	=	80	ns
th(C-Q)	TXDi hold time	0	-	ns
tsu(D-C)	RXDi input setup time	70	=	ns
th(C-D)	RXDi input hold time	90	-	ns

i = 0, 2

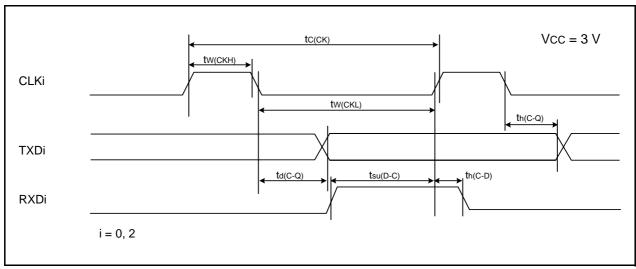


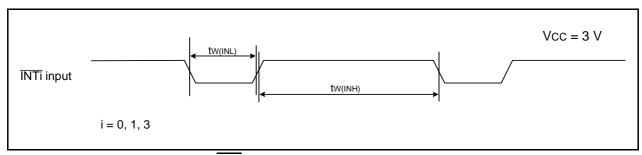
Figure 5.10 Serial Interface Timing Diagram when Vcc = 3 V

External Interrupt INTi (i = 0, 1, 3) Input **Table 5.25**

Symbol	Parameter	Stan	Unit	
Symbol	i didilictei		Max.	Offic
tw(INH)	INTi input "H" width	380 ⁽¹⁾	-	ns
tw(INL)	INTi input "L" width	380(2)	-	ns

NOTES:

- 1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.



External Interrupt INTi Input Timing Diagram when Vcc = 3 V Figure 5.11

Table 5.26 Electrical Characteristics (1) [Vcc = 2.2 V]

Symbol	Parameter		Condition		Standard			Unit
Symbol	Fair	ametei	Condition		Min.	Тур.	Max.	Unit
Vон	Output "H" voltage	Except P2_0 to P2_7, XOUT	Iон = −1 mA		Vcc - 0.5	_	Vcc	V
		P2_0 to P2_7	Drive capacity HIGH	Iон = −2 mA	Vcc - 0.5	=	Vcc	V
			Drive capacity LOW	Iон = −1 mA	Vcc - 0.5	=	Vcc	V
		XOUT	Drive capacity HIGH	Iон = -0.1 mA	Vcc - 0.5	1	Vcc	V
			Drive capacity LOW	IOH = -50 μA	Vcc - 0.5	1	Vcc	V
Vol	Output "L" voltage	Except P2_0 to P2_7, XOUT	IoL = 1 mA		-	=	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	IOL = 2 mA	-	-	0.5	V
			Drive capacity LOW	IOL = 1 mA	=	=	0.5	V
		XOUT	Drive capacity HIGH	IOL = 0.1 mA	=	=	0.5	V
			Drive capacity LOW	IOL = 50 μA	=	-	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, RXD0, RXD2, CLK0, CLK2		•	0.05	0.3	-	V
		RESET			0.05	0.15	-	V
lін	Input "H" current	•	VI = 2.2 V		-	-	4.0	μА
lıL	Input "L" current	" current			=	-	-4.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V		100	200	600	kΩ
RfXIN	Feedback resistance	XIN			-	5	-	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	I	-	V

NOTE:

^{1.} Vcc = 2.2 V at Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), f(XIN) = 5 MHz, unless otherwise specified.

Table 5.27 Electrical Characteristics (2) [Vcc = 2.2 V] $(Topr = -20 \text{ to } 85^{\circ}\text{C (N version)} / -40 \text{ to } 85^{\circ}\text{C (D version)}, \text{ unless otherwise specified.})$

Symbol	Parameter	Parameter Condition		Standard			Unit
Symbol	Farameter			Min.	Тур.	Max.	Offic
Icc	Power supply current (Vcc = 2.2 to 2.7 V) Single-chip mode, output pins are open.	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	3.5	_	mA
	other pins are Vss		XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.5	_	mA
	High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on endow supplied to socillator on endow speed on-chip oscillator o	_	3.5	_	mA		
		_	1.5	_	mA		
		on-chip oscillator	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz	_	100	230	μА
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0	_	22	60	μА
		High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	20	55	μА	
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	0.7	3.0	μΑ
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	1.1	_	μА

Timing requirements

(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at $Topr = 25^{\circ}C$) [Vcc = 2.2 V]

Table 5.28 XIN Input

Symbol	Parameter		Standard	
Symbol			Max.	Unit
tc(XIN)	XIN input cycle time	200	-	ns
twh(xin)	XIN input "H" width		-	ns
twl(XIN)	XIN input "L" width	90	-	ns

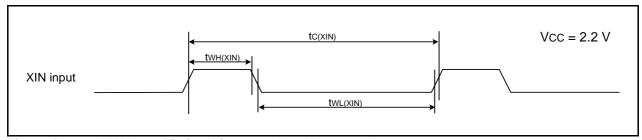


Figure 5.12 XIN Input Timing Diagram when Vcc = 2.2 V

Table 5.29 TRAIO Input

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	500	=	ns	
tWH(TRAIO)	TRAIO input "H" width	200	=	ns	
tWL(TRAIO)	TRAIO input "L" width	200	-	ns	

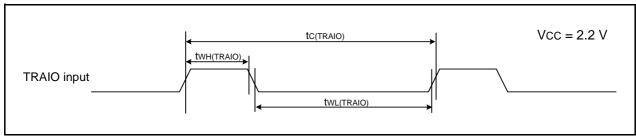


Figure 5.13 TRAIO Input Timing Diagram when Vcc = 2.2 V

Table 5.30 Serial Interface

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(CK)	CLKi input cycle time	800	-	ns	
tW(CKH)	CLKi input "H" width	400	-	ns	
tW(CKL)	CLKi input "L" width	400	-	ns	
td(C-Q)	TXDi output delay time	-	200	ns	
th(C-Q)	TXDi hold time	0	-	ns	
tsu(D-C)	RXDi input setup time	150	-	ns	
th(C-D)	RXDi input hold time	90	-	ns	

i = 0, 2

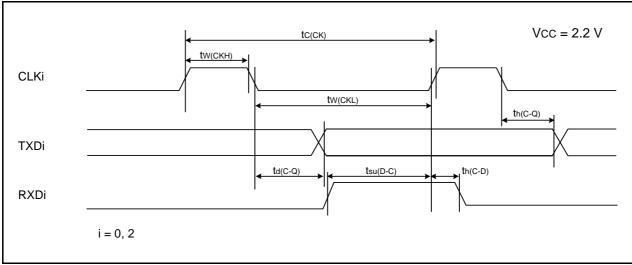


Figure 5.14 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.31 External Interrupt \overline{INTi} (i = 0, 1, 3) Input

Symbol	Parameter		Standard	
Symbol			Max.	Unit
tW(INH)	ĪNTi input "H" width	1000(1)	-	ns
tW(INL)	INTi input "L" width	1000(2)	1	ns

NOTES:

- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

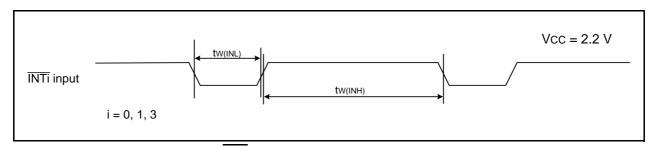
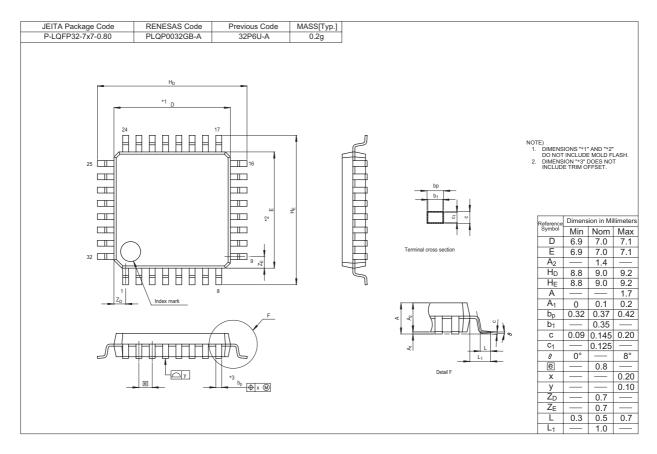


Figure 5.15 External Interrupt INTi Input Timing Diagram when Vcc = 2.2 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Technology website.



REVISION HISTORY

R8C/2K Group, R8C/2L Group Datasheet

Rev.	Date		Description
IXEV.	Date	Page	Summary
0.10	Jul 20, 2007	_	First Edition issued
1.00	Nov 07, 2007	All pages	"Preliminary" deleted
		3, 5	Table 1.2, Table 1.4;
			Current consumption: "TBD" \rightarrow "Typ. 10 mA" "Typ. 6 mA" "Typ. 2.0 μ A" "Typ. 0.7 μ A" revised
		6, 7	Table 1.5, Table 1.6 revised
			Figure 1.1, Figure 1.2; ROM number "XXX" added, NOTE1 added
		20	Table 4.4 "005Fh" "006Fh" "007Fh" "008Fh" added
		24	Table 5.2 NOTE2 revised
		32, 33	Table 5.14, Table 5.15 revised
		37, 41	Table 5.21, Table 5.27 revised
1.10	Dec 21, 2007	3, 5	Table 1.2, Table 1.4; revised, NOTE2 added
		6, 7	Figure 1.1, Figure 1.2; "Y: Operating ambient", NOTE1 added
		15, 16	Figure 3.1, Figure 3.2; "Expanded area" deleted
		17	Table 4.1 "002Ch" added, "003Bh" "003Ch" "003Dh" deleted
		20	Table 4.4 "00D4h" "00D6h" revised
		22	Table 4.6 "0143h" revised
		24	5. "The electrical characteristics" added
		31	Table 5.10 Symbol "fOCO40M": Parameter added, NOTE4 added

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